REMARKS

Claims 2, 3, 6, 15, 16, and 17 are amended for purposes of clarification and to correct inadvertent errors. No new matter has been entered and the amendment should be entered because no new search is required and the application of the prior art would not change. Claims 1-12, 14-17, and 23 are pending in this application. Reconsideration and allowance of the application are respectfully requested.

In response to the objection to claims 15-17, these claims are amended to depend from claim 1.

Claims 1-12, 14-17, and 23 are understood to be patentable under 35 USC §103(a) over "Lee" ("A Hardware-Software co-Simulation Environment," dissertation by Seungjun Lee, University of California, Berkeley, 1993) in view of "Cooke" (U.S. Patent 6,968,514 to Cooke et al.). The rejection is respectfully traversed because the Office Action does not show that all the limitations are suggested by the combination and does not provide a proper motivation for modifying the teachings of Lee with teachings of Cooke.

According to claim 1, a method for transferring data between blocks in a design during simulation includes "determining a first buffer size in response to specification of a vector input port of a first high-level block of the design; determining a second buffer size in response to specification of a scalar input port of a second high-level block of the design; ... accumulating a plurality of scalar data values received at the scalar input port in a second vector of data values that fills the second buffer size, by the second high-level block..." The second vector of data values is transferred "via a single call to the first function of the interface that couples the HLMS to the second hardware-implemented block."

Lee does not in any apparent manner consider the specification of a vector input port or a scalar input port in determining buffer sizes. The claims clearly set forth that the first buffer size is determined in response to specification of a vector input port of a first high-level block of the design, and the second buffer size is determined in response to the specification of a scalar input port of a second high-level block of the design. However, no teachings of Lee in any apparent manner correspond to these specific limitations.

The Examiner generally cites to Lee's pages 152-167 as having teachings that correspond to these limitations. These pages contain source code that implements a wrapper that encapsulates remote processes running in remote machines; a sockPort that accepts a connection request and has an I/O utility for sending and receiving a stream socket; and an interface library for a single board computer using UNIX sockets. Nothing in this source code appears to suggest that buffer sizes are determined based on a specification of a vector input port of a first high-level block of the design and a specification of a scalar input port of a second high-level block of the design. Lee contains no apparent high-level design specification of a vector input port of a block. Nor is there any apparent high-level design specification of a scalar input port of a block. Thus, there is no apparent determining of a buffer size based on the stated specifications of these input ports.

In view of the lack of apparent correspondence, and if the rejection is maintained, Applicants respectfully request that the Examiner cite to specific code segments of Lee and explain how those code segments are thought to correspond to the claimed use of the high-level design specifications of a vector input port and a scalar input port of blocks in determining the sizes of first and second buffers.

The cited teachings of Cooke does not suggest the limitations of the sizes of buffers used in transferring vectors being determined from the scalar input port and vector input port of high-level design blocks. Cooke's teachings at col. 41-42 are apparently related to designing bus bridges. Thus, there is no apparent suggestion of using the specification of either the scalar input port or the vector input port in high-level design blocks to determine the sizes of the buffers which are used during co-simulation (there being no buffer specified in an actual design created under Cooke). In view of the lack of apparent correspondence and if the rejection is maintained, Applicants respectfully request an explanation of those specific elements in Cooke's specification that are believed to correspond to these limitations.

The asserted motivation for combining Cooke with Lee is unsupported by evidence and improper. The Office Action states that "it would have been obvious ... to combine the simulation method of Cooke et al. with the co-verification system and method of Lee because Cooke et al. teaches the advantage of using a method that

provides a methodology for constructing re-usable circuit blocks which takes account of the special requirements of programmable components, and facilitates the integration of such programmable components with non-programmable components." There is no evidence presented that Lee's system is in any way deficient in the way in which programmable components may be integrated into a design. Nor does the Office Action provide any evidence that shows how specific teachings of Cooke would remedy any of Lee's deficiencies. Therefore, the asserted motivation is improper.

Independent claim 23 is an apparatus claim that includes functional limitations similar to those of claim 1 as discussed above. Claims 2-12 and 14-17 depend from claim 1 and include limitations that further refine the limitations of claim 1 as discussed above. Therefore, the Office Action has not shown that the Lee-Cooke combination suggests the limitations of claims 2-12, 14-17, and 23.

The rejection of claims 1-12, 14-17, and 23 should be withdrawn because a *prima facie* case of obviousness has not been established.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned at 720-652-3733 is invited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on October 1, 2007.

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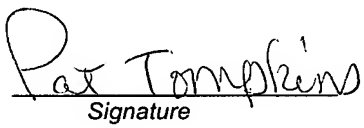

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